The formal drawings submitted by Applicant on April 23, 2001, divided Fig. 3 into Figs. 3A and 3A, and divided Fig. 2 into Figs. 2A and 2B.

To further the prosecution of this application, minor corrections have been made to the specification, a majority of which were made to properly reference the divided Figs. 2A, 2B, 3A, and 3B.

The Examiner is respectfully requested to approve these proposed corrections.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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Docket No. S1415/7009/SJH/DPM
Dated: May 22, 2001
x05/22/01

MARKED-UP SPECIFICATION

Please replace the paragraph beginning on page 8, line 10 as follows.

[Fig. 2 is] Figs. 2A and 2B are a flow chart of an illustrative embodiment of Act 6 of Fig. 1;

Please replace the paragraph beginning on page 8, line 11 as follows.

[Fig. 3 is] Figs. 3A and 3B are a flow chart of an illustrative embodiment of Act 14 of Fig. 1;

Please replace the paragraph beginning on page 9, line 23 as follows:

[Fig. 2 is] Figs. 2A and 2B are a flow chart of an illustrative embodiment of Act 6, where the first block coding scheme is 8B/10B.

Please replace the paragraph beginning on page 10 line 21 as follows:

As will be discussed in more detail below in relation to [Fig. 3] Figs. 3A and 3B, of the six bits appended to the two segments, two of the bits, for example, the first two bits, may be designated to indicate that the second sequence was formed by dividing a first sequence into two segments and appending six bits to each segment. For example, using the bits specified above, for the six bits added to each segment, the first two bits of the six bits is "01". Therefore, these two bits "01" may indicate that the second sequence was formed by dividing a first sequence into two segments and appending six bits to each segment. Although the bit combination "01" is used above, other bit combinations may be used for such an indication.

Please replace the paragraph beginning on page 11, line 17 as follows:

If, in accordance with Act 116, one of the two bits has a high logical value and one of the two bits has a low logical value, this 2-bit sequence should be selected to be different than the 2-bit sequence included in the six bits appended to a segment in Act 108. As will be described below in more detail in relation to Figs. [3] 3A, 3B and 4, when a second sequence is decoded into at least part of a first sequence, for example, by a signal decoder, two bits of the 10-bit

second sequence (e.g., the first two bits), may be examined to determine how to decode the 10-bit second sequence.

Please replace the paragraph beginning on page 13, line 20 as follows:

[Fig. 3 is] Figs. 3A and 3B are a flowchart of an illustrative embodiment of Act 14, where the first block coding scheme is 8B/10B as defined by the GE specification.

Please replace the paragraph beginning on page 15, line 13 as follows:

Although described above in relation to Figs. [1-3] 1, 2A, 2B, 3A and 3B are various techniques for encoding signaling information at a physical layer of a protocol, other information also may be encoded at the physical layer of a protocol using the same or similar techniques. For example, control words corresponding to a protocol could be encoded as a bit sequences not defined for use by the block coding scheme defined by the protocol. For example, if the block coding scheme is 8B/10B as defined by the GE specification, 10-bit code sequences not defined for use by the GE specification[,] may be used to encode control words of a signaling protocol, for example, start-of-frame end-of-frame, initiate, end session, error propagation alerts, and frame check sequences.

Please replace the paragraph beginning on page 16, line 1 as follows:

The signaling encoder 312 receives the one or more first sequences 310 and generates one or more second sequences 316, for example, by applying a signal encoding algorithm such as that described above in relation to Act 6 of Figs. 1, 2A and [2] 2B. To generate the one or more second sequences, the signaling encoder 312 may include or have access to a first LUT 314 that includes a plurality of entries. Each entry of the first LUT 314 may correspond to a possible first sequence of the one or more first sequences 310 and may contain one or more second sequences (of the one or more second sequences 316) that corresponds tot he possible first sequence.

Please replace the paragraph beginning on page 16, line 9 as follows:

The first LUT 314 may have been loaded by pre-applying a signal encoding algorithm, for example, as described in relation to Act 6 of Figs. 1, 2A and [2] 2B, to each first sequence

and storing the resulting second sequence in an entry of the first LUT 314, where the entry is assigned to the received first sequence.

Please replace the paragraph beginning on page 17, line 28 as follows.

The signaling decoder 334 receives the one or more second sequences 316 and decodes the one or more second sequences 316 to produce the one or more first sequences 310, for example, by applying a signal decoding algorithm such as that as described above in relation to Act 14 of Figs. 1, 3A and [3] 3B. To decode the one or more second sequences 316, the signaling decoder 334 may include or have access to a second LUT 336, which includes a plurality of entries. Each entry of the second LUT 336 may correspond to a second sequence of the one or more second sequences 316, and may contain a first sequence of the one or more first sequences 310 that corresponds to the second sequence.

Please replace the paragraph beginning on page 18, line 4 as follows:

The second LUT 336 may have been loaded by pre-applying a signal decoding algorithm, for example, as described in relation to act 14 of Figs. 1, 3A and [3] 3B, to each second sequence and storing the resulting first sequence (or at least part of a first sequence) in an entry of the second LUT 336, where the entry is assigned to the received second sequence.

Please replace the paragraph beginning on page 18, line 24 as follows:

Further, one of the first device or second device may be User Device (UD), which is a network device external to an Optical Transport Network (OTN), and one of the first device or second device may be a Transport Network Device (TND), which is a network device included as part of an Optical Transport Network (OTN). An OTN is a network in which all of the network transmission links between network devices are optical transmission links, for example, fiber optic cables, although one or more of the network devices, for example, OXCs and ADMs, may process the transmitted signals non-optically.

Please replace the paragraph beginning on page 18, line 32 as follows:

The system 300 is merely an illustrative example of a system for transmitting signaling information from a first device to a second device, where data transmitted between the first

device and the second device is encoded according to a first block coding scheme. Variations of the system 300 and other systems may be used to implement the methods and techniques described above in relation to Figs. [1-3] 1, 2A, 2B, 3A, and 3B.

Please replace the paragraph beginning on page 19, line 11 as follows:

To encode signaling information, or other information, as described above in relation to Figs [1-3] 1, 2A, 2B, 3A, and 3B, one or more devices, for example, the first device 302 and the second device 324 of Fig. 4, may be configured individually, or in combination, with logic to implement the encoding methods and techniques, or variations thereof, described above in relation to Figs. [1-3] 1, 2A, 2B, 3A, and 3B. Such logic may be implemented using hardware (e.g., one ore more application-specific integrated circuits), firmware (e.g., electrically-programmable logic), software, or a combination thereof. Each such one or more devices may include, among other things, a plurality of known components such as one or more processors, a memory system, a disk storage system, ore or more network interfaces connecting the device to network links that connect to network resources, components for processing (e.g., multiplexing, switching, routing, converting, etc.) network signals and data,, and one or more busses or other internal communication links interconnecting the various components.